10/709,293

IN THE CLAIMS:

Please cancel claims 1-3, 5, 8, 9, 14-17 and 19 without prejudice or disclaimer.

Please amend the remaining claims as follows:

1-3. (Cancelled).

4. (Currently Amended) ~~The method in claim 1,~~ A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

5. (Cancelled).

6. (Currently Amended) ~~The method in claim 1,~~ A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said individual fault mechanisms.

7. (Currently Amended) ~~The method in claim 1,~~ A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

wherein said constructing of said composite Voronoi diagram comprises forming a logical NOT of said individual fault mechanisms.

8-9. (Cancelled).

10. (Currently Amended) A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram ~~The method in claim 8,~~

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

11. (Currently Amended) A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram, ~~The method in claim 8,~~

further comprising computing the critical area of a logical NOT of said individual fault mechanisms in a process comprising subtracting the critical area of said individual fault mechanisms from the area of said integrated circuit.

12. (Currently Amended) ~~The method in claim 8,~~ A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

further comprising computing the critical area of a logical AND of said individual fault mechanisms in a process comprising:

adding the critical areas of a first individual fault mechanism to a second individual fault mechanism to produce an intermediate result; and

subtracting the critical area of said logical OR composite of said first individual fault mechanism and said second individual fault mechanism from said intermediate result.

13. (Currently Amended) ~~The method in claim 8,~~ A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

further comprising computing the critical area of any boolean composition of said individual fault mechanisms in a process comprising:

arranging the boolean composition into disjunctive normal form; and

computing the sums and differences of component critical areas of logical OR composites, wherin the logical OR composites contain ~~of~~ subsets of said individual fault mechanisms.

14-17. (Cancelled)

18. (Currently Amended) ~~The program storage device in claim 15,~~ A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

19. (Cancelled).

20. (Currently Amended) ~~The program storage device in claim 15,~~ A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram,

wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said individual fault mechanisms.